

REMARKS

Claims 1-34 remain pending in this application.

The Examiner rejected claims 1-34 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,877,861 (*Ausschnitt*). Applicants respectfully traverse this rejection.

In the Final Office Action dated December 2, 2005, the Examiner, again, asserted that the level-to-level overlay errors of *Ausschnitt* equates to the wafer mean error. Further, the Examiner cites page 14 of the Specification of the present application, which discloses that the wafer mean error data relates to the average overlay error for a particular wafer as a whole from one process to another. It is clear that the specification discloses the wafer mean error data relating to average overlay error for a particular wafer as a whole. In contrast, *Ausschnitt* refers to particular layers of wafers, such as level A66 to the level B60 of Figure 8. *Ausschnitt* also refers to the fact that it is directed to the absolute error relating to level A and level B. *Ausschnitt* does not disclose an average overlay error for a wafer as a whole. Therefore, the Examiner's arguments in the Final Office Action dated December 2, 2005, does not disprove Applicants' arguments, which are discussed in further details below.

Further, in the Final Office Action dated December 2, 2005, the Examiner asserted that the Applicants' Specification and claims fail to disclose a definition of wafer mean error. Applicant respectfully asserts that the claims do not need to define a wafer mean error since those skilled in the art having benefit of the present disclosure, upon reading of the claims, would readily decipher the context of the term "wafer mean error". As cited by the Examiner, the discussion regarding the term "wafer mean error data" in the Specification would allow those skilled in the art to readily decipher the meaning of the term "wafer mean error," which as

describe herein, is clearly not anticipated by *Ausschnitt*. Further, *Ausschnitt* does not make obvious various other elements of the claims of the present invention, such as comparing field mean error to a wafer mean error and performing a residual error analysis, which is not even remotely contemplated by *Ausschnitt*. These arguments are discussed in further detail below. Therefore, as described herein, various elements of the claims of the present invention are not taught, disclosed, or suggested by *Ausschnitt*.

Ausschnitt does not teach, disclose, or suggest all of the elements of claim 1 of the present invention. In the Final Office Action dated December 2, 2005, the Examiner misrepresents various terms disclosed in *Ausschnitt* to argue anticipation of various elements of claim 1. For example, the Examiner considers “level-to-level metrology” in *Ausschnitt* to be equivalent to wafer-mean error metrology analysis of the present invention. Other misapplications were also made in the Office Action, as described below. *Ausschnitt* merely discloses performing analysis of within-level overlay errors as well as of level-to-level field overlay errors. The level-to-level disclosure in *Ausschnitt* merely refers to multiple layers of the wafers, such as the “level A” 66 and the “level B” 60. *See* Figure 8, column 3, lines 44-49. *Ausschnitt* also refers to the fact that it is directed to the absolute error relating to level A and level B and not necessarily to the relative error between level A and level B. *See* column 3, lines 49-52. Applicants respectfully assert that the Examiner misunderstands the level-to-level error disclosed by *Ausschnitt*. *Ausschnitt* is clear as to the fact that the level-to-level term relates to level-to-level field overlay error and not to the wafer-mean error called for by claims of the present invention. *See* column 4, lines 56-60. In other words, *Ausschnitt* is concerned with alignment of a field in level B to a field in level A and not to the wafer-mean error called for by claims of the present invention.

Ausschnitt also refers to within-level field overlay errors. In other words, *Ausschnitt* is merely referring to checking for errors on one layer. This assertion is further bolstered by the description in block 82 of Figure 12, which determines whether if the analysis relates to a first level; if so, then the level A to level A overlay error is measured. See, Figure 12. If the analysis relates to an Nth level, then the level A to level B error is calculated. *Id.* Subsequently, the level to level error, which the Examiner mistakenly considers as being equivalent to wafer-mean error, is further described in block 86, which calls for calculating field terms after measuring the level A to level B overlay error. See Figure 12. Therefore, it is clear that the level-to-level description of *Ausschnitt* does not equate to wafer-mean error, but merely refers to overlay errors between one layer to another. Therefore, the Examiner erred in equating level-to-level metrology of *Ausschnitt*, to the wafer mean error metrology called for by claim 1 of the present invention. Therefore, Applicants respectfully assert that the element of determining a wafer-mean error is not disclosed, taught, or suggested by *Ausschnitt*.

Furthermore, the Examiner asserted that the comparison of the field-mean error to the wafer-mean error element called for by claim 1 of the present invention, is disclosed by the mere assertion in the summary of the invention relating to a description that correction factors are calculated from field-term error, alignment errors, and the level-to-level overlay measurement using the processor. Firstly, as Applicants described above, level-to-level error does not teach, disclose, or suggest wafer-mean error. Further, nowhere does *Ausschnitt* disclose comparing the field-mean error to the wafer-mean error. The mere assertion in *Ausschnitt* that the correction factors are calculated from the field-mean, field-term alignment errors and the level-to-level overlay measurements, does not equate to a comparison between the two. Therefore, the claim 1

element of comparing the field-mean error to the wafer-mean error is also not taught, disclosed, or suggested by *Ausschnitt*.

Additionally, the Examiner attempts to read upon the element of performing residual error analysis based upon the field-to-field analysis and the wafer-mean error by citing col. 6, line 39, which refers to an equation using least squares best fit technique. The Examiner also points to col. 1, line 20, referring to a mere assertion relating to keeping an alignment error between levels below acceptable product tolerance. Applicants respectfully assert that these portions of the disclosure of *Ausschnitt* do not teach, disclose, or suggest the residual error analysis called for by claim 1 of the present invention. These calculations merely refer to errors relating to a level to level (i.e., layer to layer) field error, and does not disclose or suggest the residual error analysis based upon field-to-field analysis and the wafer-mean error, as called for by claim 1 of the present invention. Nowhere does *Ausschnitt* refer to performing a residual-error analysis based upon the field-to-field analysis as well as the wafer-mean analysis. Additionally, the residual-error analysis of claim 1 includes determining whether significant residual error exists as a result of comparing the residual error with a predetermined tolerance. *Ausschnitt* does not make such comparison. The mere assertion of the alignment error between levels being below product tolerance does not read upon this limitation. Furthermore, as described above, *Ausschnitt* does not disclose a residual-error analysis being based upon a comparison between wafer-mean error and a field-mean error. First of all, as described above, *Ausschnitt* does not disclose determining a wafer-mean error. Secondly, *Ausschnitt* does not disclose or suggest determining comparing the wafer-mean error to the field-mean error. Therefore, several elements of claim 1 of the present invention are not taught, disclosed, or suggested by

Ausschnitt. Therefore, claim 1 of the present invention is allowable for at least the reasons cited above.

Furthermore, claim 11 calls for a system to determine a field-mean error and a wafer-mean error and to perform a comparison to generate modification data, which is not taught or suggested by *Ausschnitt* for at least the reasons cited herein. Claims 15 and 16 call for apparatuses to determine a field-mean error and a wafer-mean error to perform a comparison in order to determine a residual error, which are elements that are not taught, disclose or suggested by *Ausschnitt* for at least the reasons cited above. Additionally, claims 26 and 29 respectively call for a system and an apparatus for determining a field-mean error and a wafer-mean error to perform a comparison in order to determine a residual error, which are elements that are not taught, disclose or suggested by *Ausschnitt* for at least the reasons cited above. Therefore, independent claims 1, 11, 15, 16, 26, and 29 are allowable for at least the reasons cited above.

Independent claims 1, 11, 15, and 16, are allowable for at least the reasons cited above. Additionally, dependent claims 2-10, 12-14, and 17-25, which depend from independent claims 1, 11, and 16, respectively, are also allowable for at least the reasons cited above.

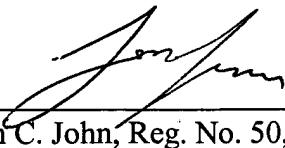
In light of the arguments presented above, Applicants respectfully assert that claims 1-34 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the **Examiner is requested to call the undersigned attorney** at the Houston, Texas telephone

number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
CUSTOMER NO. 23720

Date: February 2, 2005 By: 
Jaison C. John, Reg. No. 50,737
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-7000
(713) 934-7011 (facsimile)
ATTORNEY FOR APPLICANT(S)